PATENT

I hereby certify that this correspondence is being deposited with the United States Postal Service by facsimile addressed to: Attn: Tony Hood; Assistant Commissioner for Patents, FAX No.: 703-578-6812.
Date of Deposit: October 29th 2004
By: Laura M. Clark
Signature: Laura M. Clark

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: TED SCOTT RAKEL, ET AL.

SERIAL NO: 09/595,036 **EXAMINER: Ferris III, Fred O.**

FILED: 06/15/2000 **ART UNIT: 2128**

CONFIRMATION NO. 9158 **ATTORNEY DOCKET NO. 10992563-1**

TITLE: METHOD FOR DETERMINING THE DC MARGIN OF A LATCH

SPECIAL COMMUNICATION
THE ASSISTANT COMMISSIONER OF PATENTS
AND TRADEMARKS
WASHINGTON, D.C. 20231

SIR:

In response to the Notice of Allowance dated 08/05/2004, please correct the title of the application as follows:

The title of the application on the Notice of Allowance now reads: "MOTHOD OF DETERMINING DC MARGIN OF A LATCH".

The title of the application as filed and as listed on the specifications and accompanying documentation is: "**METHOD OF DETERMINING DC MARGIN OF A LATCH**" (emphasis added).

Please make this change to reflect the correct title of the application on the issued patent. I enclose a copy of the first page of the Application specifications filed 6/15/00 showing the correct title, as well as the transmittal page for this application and retuned postcard showing the filing date. The issue fee was paid today, October 29, 2004.

Respectfully submitted,

Ted Scott Rakel, et al.

by William P. O'Meara Oct 29, 2004
William P. O'Meara Date
Reg. No: 29,962
Agent for Applicant; (970) 898-7917

Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80528-9599

ATTORNEY DOCKET NO. 10992563-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

EL634172995US

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Ted Scott Rakel et al**

TITLE: **Method For Determining The DC Margin Of A Latch**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed
(X) 7 sheets of drawings (one set) ( ) Associate Power of Attorney
( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449
( ) Priority document(s) ( )(Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	20 — 20	0	X $18	$ 0
INDEPENDENT CLAIMS	3 — 3	0	X $78	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$260	$ 0
BASIC FEE: Design $310.00); Utility$690.00)				$ 690
			TOTAL FILING FEE	$ 690
			OTHER FEES	$
			TOTAL CHARGES TO DEPOSIT ACCOUNT	$ 690

Charge $ 690 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17,1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EL634172995US

Date of Deposit 6/15/00

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By Linda C. Cunningham

Typed Name: Linda C. Cunningham

Respectfully submitted,

Ted Scott Rakel et al

By _____

Alexander J Neudeck

Attorney/Agent for Applicant(s)
Reg. No. 41,220
Date: 6-14-00

Telephone No.: (970) 898-4931

METHOD OF DETERMINING DC MARGIN OF A LATCH

Technical Field

The invention relates to electronic circuits. More particularly, the invention relates to simulation and determination of design parameters of an electronic circuit.

Background Art

A latch is a circuit element that maintains a particular state between state changing events, i.e., in response to a particular input, and is ubiquitous in digital sequential circuit designs. For example, as shown in Fig. 1, a typical latch **100** may include, inter alia, a forward inverter **101**, a feedback inverter **102**, an input terminal **103** and an output terminal **104**. The output voltage level, V_{OUT}, remains at a particular voltage level, i.e., either high or low, until an input signal, V_{IN}, is received at the input terminal **103**, at which time the state of the output may change depending on the nature of the input signal. For example, the state of the output **104** may change from a high state to a low state upon receipt of a logical high signal at the input **103**.

In order for the latch to operate properly, i.e., to change state upon receiving a particular input, the input signal levels to the latch must exceed certain thresholds with a sufficient margin. To this end, during a circuit design, it must be ensured that the input signal levels delivered through various signal paths to each of latches in the circuit under design meet the above input signal margin.

One of the ways to ensure satisfaction of the above input signal level requirement is to determine what is often referred to as the "DC margin" for each of the latches present in the circuit being designed.